a second diffusion region, the second diffusion region couples the transistor to a bit line;

wherein the gate serves as a word line;

wherein the gate includes a buried portion and a non-buried portion, wherein the buried portion of the gate occupies the shallow transistor trench; and

wherein the buried portion of the gate is in contact with the first diffusion region.

4. (Amended) The memory cell of claim 3 wherein the first diffusion region is located in a region of the substrate between the trench capacitor and STT and an interface of STT and the substrate between the first and second diffusion regions forms a channel of the transistor.

10. (Amended) The memory cell of claim 9 wherein the gate further comprises a cap layer over the non-buried portion of the gate.

12. (Amended) The memory cell of claim 11 wherein the gate further comprises a cap layer over the non-buried portion of the gate.

REMARKS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

Claims 1, 4, 10 and 11 to more clearly and distinctly point out the subject matter applicant regards as the invention.

Claim 1 has been amended to point out that the buried portion of the gate is in contact with the first diffusion region. Such relationship is not described in Bronner, et el.

Applicant submits that all of the claims are now in condition for allowance, which action is requested. Filed herewith is a check in payment of the petition for automatic extension with the required fee